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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,897	04/20/2001	James Ma	P4785	4309

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EXAMINER	
NGUYEN, SON XUAN	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,897	MA, JAMES	
	Examiner	Art Unit	
	SON X. NGUYEN	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11,12,15-18 and 26* is/are rejected.

7)☐ Claim(s) *2-10,14,19-25 and 27-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 11-12, 13, 15-18, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe (U.S 6,021,086) in view of Kang (U.S 6,181,640).

Regarding claims 1, Joffe discloses a crossbar switch circuit, comprising: a plurality of ports (ports 1-32 of Figure 10) coupled to a bus (bus interface unit in line 9 of column 3); at least one memory element (shared memory of Figure 10) coupled to one of said plurality of ports; and a circuit (control memory of Figure 10) coupled to each of said at least one memory element.

Joffe, however, fails to disclose a circuit details for generating a write enable pulse comprising: a pulse generator for generating a pulse, said pulse tracking a leading edge of a clock signal; a write enable signal generator for generating a write enable signal; and a first logic circuit coupled to said pulse generator and said write enable signal generator for generating said write enable pulse by combining said pulse and said write enable signal.

Kang teaches the circuit (control unit of Figure 5) for generating a write enable pulse (write signal WR of Figure 5) comprising: a pulse generator (pulse generator 300 of Figure 5) for generating a pulse (pulse signal PLS of Figure 5), said pulse tracking a

leading edge of a clock signal; a write enable signal generator (write enable signal /WE of Figure 5 inherently come from write enable signal generator) for generating a write enable signal; and a first logic circuit (NOR gate NR520 of Figure 5 combining write enable signal /WE from ND1 and pulse signal PLS from pulse generator 300) coupled to said pulse generator and said write enable signal generator for generating said write enable pulse (write signal WR) by combining said pulse and said write enable signal.

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Joffe's apparatus to incorporate a setup where a circuit generating a write enable pulse comprising a pulse generator, a write enable signal generator and a first logic circuit for generating write enable pulse by combining pulse and write enable signal, the motivation being that using circuit for generating write enable pulse would be capable of writing correct data to memory cell and destination cell.

Regarding claims 11 and 12, Joffe discloses at least one memory element comprises a RAM (shared memory SRAM of Figure 10). Joffe does not teach RAM comprising an asynchronous RAM. However, the examiner takes Official Notice that it is old and well known in the art to have RAM comprising an asynchronous RAM. Therefore, it would have been obvious for one of ordinary skill at the time of invention to include an asynchronous RAM as memory.

Regarding claim 13, Joffe discloses a first port of said plurality of ports comprises a plurality of memory elements (memory access buffers of Figure 10), further

comprising a first selector (interconnection matrix) coupled to said plurality of memory elements, said first selector being coupled to said bus.

Regarding claims 15, Joffe discloses a computer system comprising: crossbar switch comprising: a plurality of ports (ports 1-32 of Figure 10) coupled to a bus (bus interface unit in line 9 of column 3); at least one memory element (shared memory of Figure 10) coupled to one of said plurality of ports; and a circuit (control memory of Figure 10) coupled to each of said at least one memory element; and at least one processing unit (lines 16-21 of column 1) coupled to each of said plurality of port.

Joffe, however, fails to disclose a circuit details for generating a write enable pulse comprising: a pulse generator for generating a pulse, said pulse tracking a leading edge of a clock signal; a write enable signal generator for generating a write enable signal; and a first logic circuit coupled to said pulse generator and said write enable signal generator for generating said write enable pulse by combining said pulse and said write enable signal.

Kang teaches the circuit (control unit of Figure 5) for generating a write enable pulse (write signal WR of Figure 5) comprising: a pulse generator (pulse generator 300 of Figure 5) for generating a pulse (pulse signal PLS of Figure 5), said pulse tracking a leading edge of a clock signal; a write enable signal generator (write enable signal /WE of Figure 5 inherently come from write enable signal generator) for generating a write enable signal; and a first logic circuit (NOR gate NR520 of Figure 5 combining write enable signal /WE from ND1 and pulse signal PLS from pulse generator 300) coupled to

said pulse generator and said write enable signal generator for generating said write enable pulse (write signal WR) by combining said pulse and said write enable signal.

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Joffe's apparatus to incorporate a setup where a circuit generating a write enable pulse comprising a pulse generator, a write enable signal generator and a first logic circuit for generating write enable pulse by combining pulse and write enable signal, the motivation being that using circuit for generating write enable pulse would be capable of writing correct data to memory cell and destination cell.

Regarding claims 16-18, Joffe discloses the computer system of claim 15; wherein said at least one processing unit comprises a processing unit selected from the group consisting of CPUs (central processing units) and I/O (input/output) processors; wherein a plurality of processing units are coupled to a first port, further comprising a selector for selecting one processing unit from said plurality of processing units; wherein said processing unit is an I/O (input/output) processor, further comprising an I/O buffer coupled between said port and said I/O processor (see lines 16-21 of column 1).

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atac at el. (U.S 4,985,830) in view of Kang (U.S 6,181,640).

Regarding claims 26, Atac discloses a method for communicating between a first processing unit (first processor 16 of Figure 1) coupled to a first port (first spigot of Figure 1 and 2) of a crossbar switch (bus switch of Figure 1) and a second processing

unit (second processor of Figure 1) coupled to a second port (second spigot of Figure 1 and 2) of said crossbar switch, comprising: generating a request for a communication path from said first processor to said second processor; transmitting data from said second processor to said first port (see lines 65-67 of column 15);

Atac, however, fails to disclose storing said data in a memory element in said first port, comprising: generating a pulse in response to a clock signal, said pulse tracking a leading edge of said clock signal; generating a write enable signal; and generating a write enable pulse by combining said pulse and said write enable signal;
And reading said data from said memory element.

Kang teaches storing said data in a memory element in said first port, comprising: generating a pulse in response to a clock signal (pulse generator 300 of Figure 5), said pulse tracking a leading edge of said clock signal; generating a write enable signal (write enable signal /WE of Figure 5); and generating a write enable pulse by combining said pulse and said write enable signal (NOR gate NR520 of Figure 5 combining write enable signal /WE from ND1 and pulse signal PLS from pulse generator 300); and reading said data from said memory element (see lines 17-18 of column 1).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Atac's method to incorporate a setup where data is stored in a memory element by generating a write enable pulse by combining said pulse

and said write enable signal, the motivation being that storing data by generating write enable pulse would be capable of writing correct data to memory cell and destination cell.

Allowable Subject Matter

4. Claims 2-10, 14, 19-25, 27-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Masayuki Ohtawa (U.S 5,130,979), Frame converter using a dual-port random access memory.

b) Kubo; Takashi (U.S 6,215,726), Semiconductor device with internal clock generating circuit capable of generating internal clock signal with suppressed edge-to-edge jitter.

c) Chiou at el. (US 6577625), Ethernet switch with a share memory structure and method for sharing memory.

d) Brown; David A (US 6,711,170), Method and apparatus for an interleaved non-blocking packet buffer.

e) Gorshe at el. (U.S 5,878,039) Bus rate adaptation and time slot assignment circuit for a sonet multiplex system.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SON X. NGUYEN whose telephone number is 571-272-6048. The examiner can normally be reached on 8 AM -5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICKY NGO
PRIMARY EXAMINER